IN THE CLAIMS

The following claim set replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device, which comprises a capacitor on a semiconductor substrate, said capacitor comprising a lower electrode layer, a ferroelectric layer and an upper electrode layer, wherein a convex or concave region is formed on ~~the~~ an upper surface of the ferroelectric layer, and an upper surface of the semiconductor substrate on which the capacitor is formed being flat.

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2. (Original) The semiconductor device according to claim 1, wherein the convex or concave region formed on the upper surface of the ferroelectric layer is thoroughly covered with the upper electrode layer.

3. (Original) The semiconductor device according to claim 1, wherein a convex or concave region is formed also on the upper surface of the lower electrode layer.

4. (Original) The semiconductor device according to claim 3, wherein the convex or concave region formed on the upper surface of the ferroelectric layer is thoroughly covered with the upper electric layer, and the convex or concave region formed on the upper surface of the lower electrode layer is thoroughly covered with the ferroelectric layer.

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5. (CURRENTLY AMENDED) The semiconductor device according to claim 1, wherein a height or a depth of the convex concave region formed on the upper surface of the ferroelectric layer is not greater than half ~~or smaller than the~~ a thickness of the

ferroelectric layer, and is ~~in a range from the same as to~~ at least half a ~~the~~ thickness of the upper electrode layer.

6. (Previously Presented) The semiconductor device according to claim 1, wherein a height or a depth of the convex or concave region formed on the upper surface of the ferroelctric layer is half or smaller than the thickness of the ferroelectric layer, and is in a range from the same as to half the thickness of the upper electrode layer, and a height or a depth of the convex or concave region formed on the upper surface of the lower electrode layer is half or smaller than the thickness of the lower electrode layer, and is in a range from the same as to half the thickness of the ferroelectric layer.

7. (Original) A process for manufacturing a semiconductor device which has a capacitor comprising a lower electrode layer, a ferroelectric layer and an upper electrode layer, which comprises a step of forming a convex or concave region on the upper surface of the ferroelectric layer so that the upper electrode layer thoroughly covers the convex or concave region formed on the upper surface of the ferroelectric layer.

8. (Original) The process for manufacturing a semiconductor device according to claim 7, which further comprises a step of forming a convex or concave region also on the upper surface of the lower electrode layer so that the ferroelectric layer thoroughly covers the convex or concave region formed on the upper surface of the lower electrode layer.

9. (NEW) A semiconductor device, which comprises a capacitor comprising a lower electrode layer, a ferroelectric layer and an upper electrode layer, the ferroelectric layer having a ferroelectric layer upper surface and the upper electrode having an upper electrode upper surface, wherein a convex or concave region is formed on the upper surface of the ferroelectric layer in a manner such that a non-smooth region on the

ferroelectric layer upper surface is not aligned, in a direction perpendicular to a thickness of the ferroelectric layer, with a non-smooth region on the upper electrode upper surface.

10. (New) The semiconductor device according to claim 9, wherein the convex or concave region formed on the upper surface of the ferroelectric layer is thoroughly covered with the upper electrode layer.

11. (New) The semiconductor device according to claim 9, wherein a convex or concave region is formed also on the upper surface of the lower electrode layer.

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12. (New) The semiconductor device according to claim 11, wherein the convex or concave region formed on the upper surface of the ferroelectric layer is thoroughly covered with the upper electric layer, and the convex or concave region formed on the upper surface of the lower electrode layer is thoroughly covered with the ferroelectric layer.

13. (New) The semiconductor device according to claim 9, wherein a height or a depth of the convex concave region formed on the upper surface of the ferroelectric layer is not greater than half a thickness of the ferroelectric layer, and is at least half a thickness of the upper electrode layer.

14. (New) The semiconductor device according to claim 9, wherein a height or a depth of the convex or concave region formed on the upper surface of the ferroelctric layer is half or smaller than the thickness of the ferroelectric layer, and is in a range from the same as to half the thickness of the upper electrode layer, and a height or a depth of the convex or concave region formed on the upper surface of the lower electrode layer is half or smaller than the thickness of the lower electrode layer, and is in a range from the same as to half the thickness of the ferroelectric layer.